

Network on Chip and Its Low Power Techniques

Premalatha P¹, Dr. Paramasivam K²

¹Research Scholar, Department of EEE, Kumaraguru College of Technology, Coimbatore, Tamilnadu, India.

²Professor, Department of EEE, Kumaraguru College of Technology, Coimbatore, Tamilnadu, India.

To Cite this Article: Premalatha P¹, Dr. Paramasivam K², “Network on Chip and Its Low Power Techniques”, Indian Journal of Computer Science and Technology, Volume 03, Issue 02 (May-August 2024), PP: 55-59.

Abstract: The advent of Network-On-Chip (NoC) architecture has significantly revolutionized the design of complex System-On-Chip (SoC) systems by providing scalable and efficient communication infrastructures. NoC architectures offer advantages such as high bandwidth; low latency and better scalability compared with traditional bus-based communication architectures. However, the ever-increasing demand for higher performance and lower power consumption poses significant challenges for NoC designers. This article reviews the basic architectures and design issues of NoCs with SoCs and further extended with research challenges and low power techniques.

Key Words: Network-On-Chip, System-On-Chip, latency and scalability.

I.INTRODUCTION

Due to transistor scaling, IC packaging density doubles each year as stated by Moore’s law. These advancements lead VLSI integration towards nano scale era, witnessed a shift from computation centric designs to communication centric designs incorporating massive amount of simple cores. The typical interconnect schemes like point to point, buses and crossbars are existing for minimal number of cores. Wire density becomes a barrier in point to point topology for adapting them to many core architectures. Scalability and arbitration issues in conjunction with bandwidth bottleneck make bus topology viable to many core architectures. Area and power requirements limit crossbars applicability. Hence, efficient communication infrastructure like Network-On-Chip (NoC) is emerged to handle the communication challenges. The key features are listed:

- NoC possess bandwidth scaling with minimal power and area overheads.
- Quality of service and higher bandwidth can be achieved through multiplexing traffic through same channel.
- Iterative blocks make the verification process simple.

II.SYSTEM ON CHIP

Reduced design manufacturing time, specified by the customers, makes full-custom design incompatible and has led to the Intellectual Property (IP) cores design. With the adverse design complexity, a single-chip implementation that integrates many IP cores performing a range of functions and operating at diverse clock ranges is possible through System-On-Chip (SoC) technology.

SoCs are broadly classified into two categories based on usage and flexibility:

- (1) General-Purpose Multi Processor SoC (MPSoC) and
- (2) Application-Specific SoC. The SoC architecture consists of a processor, DSP, memory, network interface card, CPU, multimedia encoder/decoder, DMA, etc.

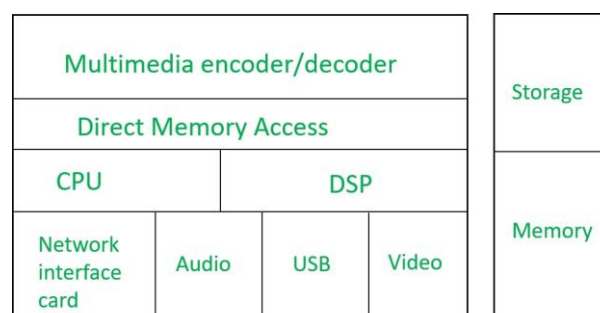


Fig 1.1 SoC Architecture

Processor:

The CPU is the primary processing unit of the SoC, responsible for executing instructions and performing computations. It may consist of one or multiple processor cores, each capable of executing instructions independently.

DSP:

it is included in SoC to perform signal processing operations such as data fetching and data processing, etc.

Memory:

SoCs typically include various types of memory, including RAM (Random Access Memory) for temporary data storage and ROM (Read-Only Memory) for storing firmware or boot code. Additionally, SoCs may incorporate caches to improve memory access speed.

Encoder/Decoder:

interrupts information and converting it into codes.

Network Interface card:

SoCs feature internal interconnects that facilitate communication between different components within the chip. These interconnects may include buses, crossbars, or networks-on-chip (NoCs) to efficiently manage data transfer between components.

GPU:

Graphical Processing Unit, used to establish interface. It is intended to speed up image calculations.

Peripheral devices:

Externally connected devices /interfaces such as USB, HDMI, Wi-Fi, and Bluetooth are incorporated in peripheral devices to perform consumer operations.

UART:

This block is used to transmit or receive serial data. Voltage regulators, Oscillators, clocks, and ADC/DAC are also part of SoC.

III. LIMITATIONS IN SOC

System on Chip (SoC) technology has revolutionized the design and development of various electronic devices, integrating multiple functionalities onto a single chip. However, like other technology, SoCs have their boundaries. Some of these limitations include:

Complexity: As SoC combine multiple components onto a single chip, they become increasingly complex to design, verify, and test. Managing this complexity can be challenging and may lead to longer development cycles.

Power Consumption: Integrating multiple components onto a single chip can lead to greater power consumption, especially if those components operate at different voltages or have diverse power requirements.

Thermal Management: The compact nature of SoC can lead to heat concentration, which may require complicated thermal management techniques to avoid extensive heating and to guarantee reliable operation.

Cost: While SoC can reduce the overall cost of a system by integration of components, the initial design and fabrication costs can be significant. Additionally, custom designing for specific applications may involve substantial investment.

Flexibility and Upgradability: Once fabricated, making changes or upgrades to its functionality can be challenging.

Manufacturing Yield: Fabricating SoCs with high yields can be challenging owing to their complexity.

Security: SoCs are vulnerable to security threats, including hardware-level attacks such as side-channel attacks, reverse engineering, and tampering. Ensuring the security of SoCs requires robust hardware and software measures.

Performance Bottlenecks: While SoCs integrate multiple components onto a single chip, performance bottlenecks can occur, mainly if the components have diverse performance characteristics or if the chip's interconnects cannot handle the data throughput efficiently.

IV. SOC TO NOC EVOLUTION

Academia and industry have started to reveal the communication network of future multi core system to fix emerging many-core communication demands. Point-to-Point dedicated links can be a better choice for number of cores in a SoC in response to traffic capacity, delay and power cost. Hence, significant increase in number of links observed as the number of cores increases leading to routing problem. Crossbar switch controls certain manifolds of buses. Further, interconnecting multiple cores

to a solitary switch is not efficient as it is not scalable.

Researchers have embarked on efficient platform-based methods to design the communication framework of MPSoC. On-chip network is a key to combine IPs in compound SoCs. Network-on-chip came up as the feasible choice in shaping flexible and expandable communication structures.

V. NOC ARCHITECTURE

The idea of on-chip network adopted from off-chip interconnection networks where a particular router is implemented per chip. The bandwidth of off-chip networks has lower bandwidth is typically lower than on-chip networks. Off-chip networks incur one additional pin as extra bit added. This influences the latency and annoys the synchronization problem. The beginning of on-chip networks in SoC design is the development of bus interconnects technology [R4].

IP cores establish connections among themselves through the router-based network. A core is coupled to a router via Network Interface (NI) module. The network initiates packet-switched on-chip communication between routers, whereas the NI enables flawless transmission between a range of cores and networks. Thus evaporates the need for global synchronization.

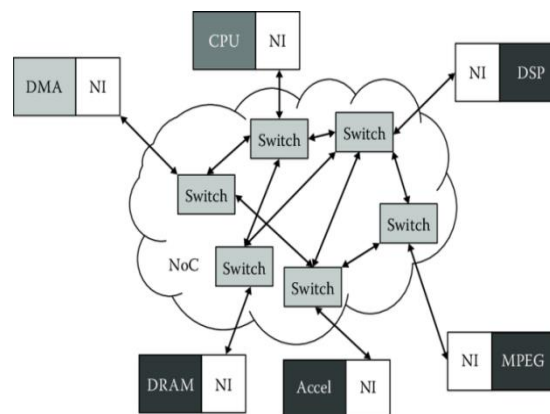


Fig 1.2 NoC Architecture

Fig 1.2 exhibits NoC structure. NI separates the computation from communication. The network holds routers and links for point-to-point communication. Switches transmit the packets from the sender node to the receiver node as per the network topology and routing strategy. The links should be small to reduce interconnect delay. To meet market requirements and ease design productivity gap, IP cores and the bus interface protocol are extensively reused.

While reusing is another major issue that IC design firm attempt to solve, reuse of IPs, NI, and communication framework like routers, mesh, and flow control procedures can be preferred in the NoC model. While choice of mesh topology and router design is entirely customized, reusing shall not yield the ideal outcome. Therefore, reuse concept is restricted to a specific type of applications.

NoC implies quite a few abstraction layers such as physical, data link, network, and transport layers, which are described as follows [R3]:

- Physical layer make a decision on the quantity and length of wires connecting resources and switches.
- Data link layer establish the communication among resources and switches. Both the physical and data link layers are dependent on technology.
- Network layer specifies the way in which a packet is delivered over the network from an absolute sender to an absolute receiver headed by recipient network address.
- Transport layer is free from technology constraints and varies the message length based on the requirement. This layer splits the message into network layer packets.

VI. LOW-POWER TECHNIQUES IN CHIP DESIGN

As conservation of energy becomes supreme in mobile, IoT, and edge computing applications, low-power design techniques play a crucial role in chip architecture. Some of them are listed below.

1. Power-Aware Routing Algorithms: Routing algorithms considerably impact power consumption in NoCs. Power-aware routing algorithms aim to lower energy consumption by reviewing traffic patterns, link utilization, and network congestion factors [R4].

2. Dynamic Voltage and Frequency Scaling (DVFS): DVFS is a broadly adopted technique for power optimization in NoC architectures. By tailoring the operating voltage and frequency of network components according to workload and traffic conditions, DVFS ensures minimum required power level with better performance. This technique effectively balancing power consumption with system demands leading to significant energy savings [R6].

3. Clock Gating and Power Gating: Clock gating and power gating are potential techniques for lowering static and dynamic power consumption in NoC designs. By conditionally disabling clock signals or halting power to components that are not in use, these techniques minimize power expenditure during periods of idle.

4. Energy-Efficient Link Design: The design of on-chip communication links drastically alters power consumption in NoC architectures, techniques such as voltage scaling, adaptive link width, and data encoding schemes optimize energy while maintaining trustworthy data transmission.

5. Topology Optimization: NoC topology plays a vital role in shaping power consumption and performance. Techniques such as hierarchical routing, mesh reshaping, and asymmetric topologies reduce communication distance and contention, thereby achieving reduced power consumption in NoC implementations.

6. Sleep Modes and Dynamic Resource Allocation: Combining sleep modes and dynamic resource allocation mechanisms in NoC architectures allows effective utilization of network resources while downplaying power consumption. Introducing low-power sleep states, during periods of inactivity and by allocating bandwidth and buffer resources based on real-time traffic demands, ensuring optimal performance with minimal power overheads.

By implementing these techniques and strategies, researchers aim to address power consumption challenges in network on chip architectures and enhance the energy efficiency and performance of on-chip communication systems.

VII. NOC OVER SOC

Networks-On-Chip (NoCs) addresses the energy and performance demands, and scaling of Systems-On-Chip (SOCs) in following ways:

1. Power Efficiency:

NoCs offer improved power efficiency compared to customary bus-based interconnects. By employing shared links and permitting high levels of parallelism, NoCs can improve performance while minimizing power consumption [R4].

2. Performance Enhancement:

NoCs provide superior performance and scalability by allowing simultaneous operation of multiple links on different data packets. This concurrent operation capability raises throughput and overall system performance [R4].

3. Scalability:

NoCs are designed to scale efficiently as the system size grows. The topology of a NoC allows for the addition of links as needed, guaranteeing that the communication infrastructure can expand along with the system requirements [R3].

4. Decoupling Communication from Computation:

NoCs detach communication from computation, in which the separation allows for more efficient data transfer and communication between IP cores [R3].

5. Flexibility and Modularity:

NoCs offer flexibility and modularity, allowing for simple integration of IP cores created by diverse entities. This modularity enables the establishment of custom network topologies personalized to specific application requirements [R3].

6. Improved Design Productivity:

By providing a structured and controlled communication network, NoCs enhance engineering productivity. They support modularity, IP reuse, and system test capabilities, making the design process more efficient [R3].

7. Adaptation of Networking Concepts:

NoCs influence concepts from packet-switched networks and tailor them to on-chip communication. This adaptation allows for the application of communication theory and methods to optimize on-chip interconnections [R3].

VIII. RESEARCH ISSUES IN NOC DEVELOPMENT

Network on Chip technology has vibrant research scope with abundant consumer applications in industry as it is anticipated to be a competent communication alternate of modern many-core SoCs. Various challenges in low power techniques employed in NoCs include:

1. Process Limitations:

The biggest challenges in implementing innovative interconnect paradigms in NoCs are process limitations. [R5].

2. Thermal Concerns:

The current state of technology confines the stacking of multiple logic layers in a package due to thermal concerns. Researchers are exploring thermal-aware 3D NoC architectures to ease these issues [R1].

3. Technology Limitations:

While nanophotonics-based NoCs have shown promise, the technology boundaries have barred their full realization. More work is considered necessary on the design cycle before nanophotonics NoCs are customized [R2].

4. Integration Challenges:

Integrating complex design strategies with interconnect paradigms to limit NoC power usage can be demanding. Improving traffic management and signaling strategies while integrating them efficiently is vital for effective power reduction [R5].

5. Hybrid Designs:

Implementing hybrid designs that merge wireless and wired interconnects for long-distance on-chip transmissions poses challenges. Further advancements in technology, such as carbon nanotube antennas, are needed to overcome current limitations [R5].

These challenges highlight the complexity and ongoing research efforts mandatory to fix power consumption issues in NoCs and advance low-power techniques in on-chip communication systems.

IX. SUMMARY

Network on Chip (NoC) and low-power techniques represent two cornerstones of modern chip design, offering scalability, performance, and energy efficiency in an increasingly interconnected world. By taking up the synergy between these two paradigms, semiconductor engineers are poised to unlock new frontiers in computational capability while justifying the environmental footprint of digital systems.

REFERENCES

1. Muhammad Raza Naqvi, "Low power network on chip architectures: A survey", *Computer Science and Information Technologies*, Vol. 2, No. 3, November 2021, pp. 158-168.
2. Ahmed Ben Achballah , Slim Ben Othman and Slim Ben Saoud, "Problems and challenges of emerging technology networks –on –chip: A review", *Microprocessors and Microsystems* 53 (2017) 1–20.
3. K. Paramasivam, "Network On-Chip and Its Research Challenges", *ICTACT Journal on Microelectronics*, July 2015, Volume: 01, Issue: 02 83-87.
4. Fardin Mohammadi Darvandi , Mohammad Trik , Danial Hoderaji and Kumarth Nazari , " A study on Low-power challenges in NOC", *IJSET - International Journal of Innovative Science, Engineering & Technology*, Vol. 2 Issue 8, July 2015.
5. Mark Buckler, Wayne Burleson and Greg Sadowski, "Low-power Networks-On-Chip: Progress and Remaining Challenges", *Symposium on Low Power Electronics and Design*, 132-134, 2013.
6. Fensch, C. et al., "Designing a Physical Locality Aware Coherence Protocol for Chip-Multiprocessors" *IEEE Tr. Computers*, 2013.
7. Wen-Chung Tsai, Ying-Cherng Lan, Yu-Hen Hu and Sao-Jie Chen, "Review Article ON Networks on Chips: Structure and Design Methodologies", *Journal of Electrical and Computer Engineering*, Volume 2012, 15 pages.
8. Viswanathan N, K. Paramasivam and K. Somasundaram, "Exploring Optimal Topology and Routing Algorithm for 3D Network on Chip", *American Journal of Applied Sciences* 9 (3): 300-308, 2012.